WHAT IS CLAIMED IS:

1. A differential line driver comprising:

first, second, third and fourth cascode transistors driven by a first voltage, wherein drains of the first and third transistors are connected to a first output of the differential line driver, and wherein drains of the second and fourth transistors are connected to a second output of the differential line driver;

first, second, third and fourth switching transistors connected in series with corresponding first, second, third and fourth cascode transistors and each driven by a corresponding data signal; and

first and second compound transistors inputting a control signal to control output currents of the compound transistors,

wherein the first compound transistor is connected to sources of the first and second switching transistors,

wherein the second compound transistor is connected to sources of the third and fourth switching transistors, and

wherein the first compound transistor includes first, second and third field effect transistors (FET's) connected in series with each other and with sources of the first and second switching transistors, and a fourth FET connected across the second FET, a gate of the fourth FET driven by the class AB operation signal.

2. The line driver of claim 1, wherein the control signal is a class AB operation signal.

3. The line driver of claim 1, wherein the second compound transistor includes fifth, sixth and seventh FET's connected in series with each other and with sources of the third and fourth switching transistors and an eighth FET connected across the sixth FET, a gate of the eighth FET driven by the control signal.

4. The line driver of claim 1, wherein an effective channel length of the first compound transistor changes based on the control signal.

5. The line driver of claim 1, wherein an effective channel length of the first and second compound transistors is variable.

6. A differential line driver comprising:

first, second, third and fourth cascode transistors driven by a first voltage, wherein drains of the first and third transistors are connected to a first output of the differential line driver, and wherein drains of the second and fourth transistors are connected to a second output of the differential line driver;

first, second, third and fourth switching transistors connected in series with corresponding first, second, third and fourth cascode transistors and each driven by a corresponding data signal; and

first and second compound transistors inputting a control signal to control output currents of the compound transistors and their effective channel widths,

wherein the first compound transistor is connected to sources of the first and second switching transistors, and

wherein the second compound transistor is connected to sources of the third and fourth switching transistors.

7. The line driver of claim 6, wherein total charge injected at a bias terminal of the first compound transistor is substantially zero.

8. A differential line driver comprising:

first and second half-cells, the half-cells cross connected to positive and negative differential outputs, each half-cell including:

first and second cascode transistors;

first and second switching transistors connected in series with the first and second cascode transistors and each driven by a corresponding data signal; and

a compound transistor inputting a control signal to change its output current and its aspect ratio, and connected to sources of the first and second switching transistors.

9. The line driver of claim 8, wherein the compound transistor includes first, second and third FET's connected in series with each other and with sources of the first and second switching transistors, and a fourth FET connected across the second FET, a gate of the fourth FET driven by the class AB signal.

10. A differential line driver comprising:

first and second half-cells, the half-cells cross connected to positive and negative differential outputs, each half-cell including:

first and second cascode transistors;

first and second switching transistors connected in series with the first and second cascode transistors and each driven by a corresponding data signal; and

a compound transistor inputting a control signal to change its output current and its an effective channel length, and connected to sources of the first and second switching transistors.

11. The line driver of claim 10, wherein total charge injected at a bias terminal of the first compound transistor is substantially zero.

12. A differential line driver comprising:

a plurality of cascode transistors connected to corresponding polarity outputs of the differential line driver;

a plurality of switching transistors connected in series with corresponding cascode transistors; and

a plurality of compound transistors inputting a class AB operation signal at their gates to control their common mode output current to range from 20 mA to 10 mA, and connected in series with corresponding switching transistors.

13. A differential line driver comprising:

a plurality of switching transistors connected to corresponding polarity outputs of the differential line driver; and

a plurality of compound transistors inputting a class AB operation signal at their gates to control their common mode output current to range from 20 mA to 10 mA, and connected in series with corresponding switching transistors.